AMT Semiconductors Ltd.

AMT4432

Low-power Stereo Audio Codec.

Features

- Low-power
  - 15mW stereo 48KHz playback with 3.3V analog power supply
  - Analog: 2.7V-3.6V
  - Digital Core: 1.65V-1.95V
  - Digital I/O: 1.1V-3.6V
  - -40°C to 85°C temperature range
- Ultra-low-power mode with passive analog bypass
- Stereo audio DAC:
  - 92dBA signal-to-noise ratio
  - Supports rates from 8KHz to 96 KHz
  - Digital signal processing and noise filtering available during record
- Ten audio input pins:
  - Programmable in single-ended or fully differential configurations
  - 3-state capability for floating input configurations
- Seven audio output drivers:
  - Stereo fully differential or single-ended headphone drivers
  - Fully differential stereo line outputs
  - Fully differential mono output
- Automatic gain control for record
- Communication interfaces
  - Control SPI or I2C
  - Audio serial data bus supports I2S, left- and right justified, DSP, and TDM modes
- Concurrent digital microphone and analog microphone support available

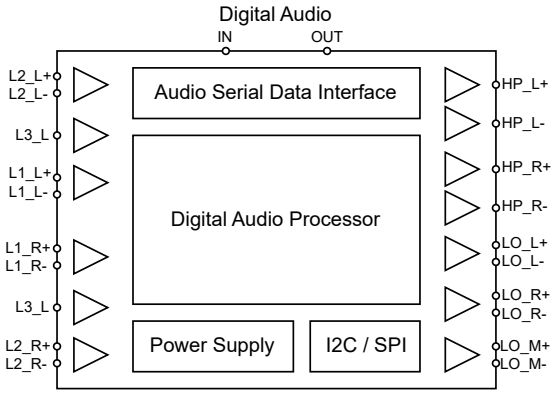
Description

The AMT4432 device is a low-power stereo audio codec with stereo headphone amplifier, as well as multiple inputs and outputs programmable in single-ended or fully differential configurations. Extensive register-based power control is included, enabling stereo 48KHz DAC playback as low as 15mW from a 3.3V analog supply, making it ideal for portable battery-powered audio and telephony applications.

Device Information

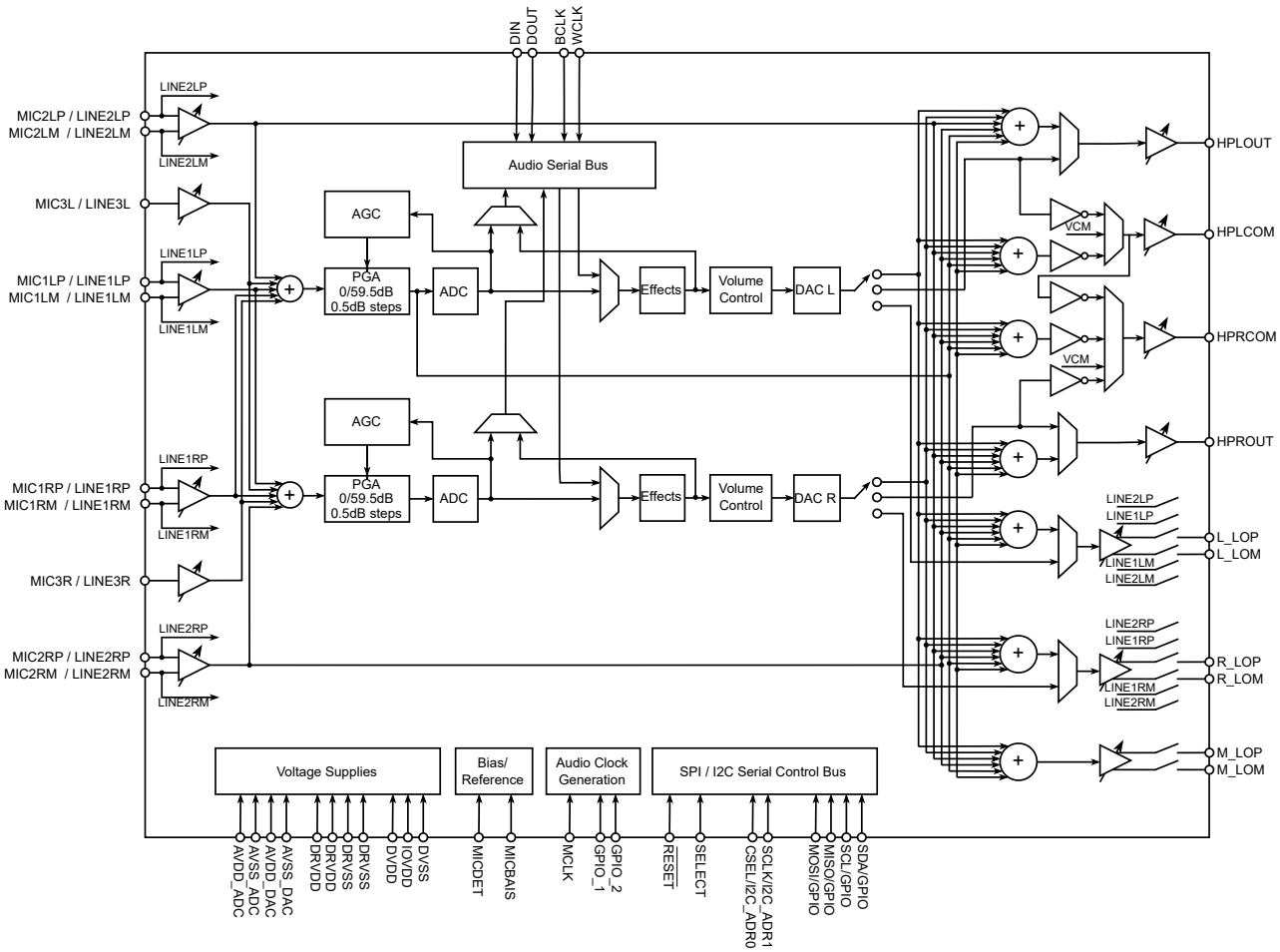
Part Number	Package	Size, mm
AMT4432	UFQFPN-48	7x7

Typical Application



AMT4432 Functional Diagram

Figure 1. AMT4432 block diagram



Functional Overview

Overview

The AMT4432 is a highly flexible, power-efficient, and feature-rich stereo audio codec designed for smartphones, PDAs, notebooks, and communications and entertainment systems. Available in 7x7mm 48-lead QFN packages, it offers a variety of features to reduce cost, board area, and power consumption in battery-powered portable devices where space is limited.

The AMT4432 consists of the following blocks:

- Multi-bit delta-sigma stereo audio DAC (8–96KHz)
- Multi-bit delta-sigma stereo audio ADC (8–96KHz)
- Programmable digital audio effects processing (3D, bass, treble, midrange, EQ, notch, de-emphasis)
- Six audio inputs
- Four powerful audio output drivers (with headphone capability)
- Three fully differential line-out drivers
- Fully programmable PLL
- Headphone/headset jack detection with interrupt

Communication with the AMT4432 for control is selected via the SELECT pin (SPI) or I2C. The SPI interface requires the slave select signal (MFP0) to be set low for communication with the AMT4432. Data is then transferred to or from the AMT4432 under the control of the host microprocessor, which also provides the serial data clock. The I2C interface supports both standard and fast communication modes, and allows up to four codecs to be cascaded onto a single I2C bus by using two addressing pins (MFP0, MFP1).

Hardware reset

The AMT4432 requires a hardware reset after power-on to operate correctly. After all power supplies have reached their specified values, the RESET pin must be driven low for at least 10 ns. If this reset sequence is not performed, the AMT4432 may not respond correctly to register read/write operations.

Digital Audio Data Serial Interface

Audio data is transferred between the host processor and the AMT4432 via a serial digital audio data interface (audio bus). The device's audio bus features a high degree of flexibility, including left- or right-justified data, support for I2S and PCM protocols, programmable data length, TDM mode for multi-channel operation, flexible master/slave mode configuration for each bus clock line, and the ability to directly interface with multiple devices in the system.

Audio Clock Generation

The audio converters in the AMT4432 require an internal clock signal of 256 × $f_{S(ref)}$, which can be derived in various ways from an external clock signal supplied to the device.

Stereo Audio ADC

The AMT4432 includes a stereo audio ADC that uses a delta-sigma modulator with 128x oversampling in single-frequency mode, followed by a digital decimation filter. The ADC supports sampling rates from 8 to 48KHz in single-frequency mode and up to 96KHz in dual-frequency mode. The ADC or DAC requires an audio drive signal and the appropriate audio generation setup when operating.

Stereo Audio ADC High-Pass Filter

In audio applications, it is often necessary to remove the DC offset from the converted audio stream. The AMT4432 has a programmable first-order high-pass filter that can be used for this purpose. The digital filter coefficients are 16-bit, so two 8-bit registers are used for each of the three coefficients, N0, N1, and D1. The transfer function of the digital high-pass filter is:

$$H(z) = \frac{N0 + N1 \times z^{-1}}{32768 - D1 \times z^{-1}}$$

Automatic Gain Control (AGC)

The Automatic Gain Control (AGC) circuit is part of the ADC and can be used to maintain a nominally constant output signal amplitude when recording speech signals (it can be completely disabled if necessary). This circuit automatically adjusts the PGA gain when the input signal becomes too loud or too weak, for example when a person speaking into the microphone moves closer to or further away from the microphone. The AGC algorithm has several programmable settings, including a target gain, attack and release time constants, noise threshold, and maximum allowable PGA gain, allowing the algorithm to be fine-tuned for any particular application. The algorithm uses the absolute mean value of the signal (which is the average of the absolute value of the signal) as a measure of the nominal amplitude of the output signal.

Note that each ADC channel has a fully independent AGC circuit with fully independent algorithm control from channel to channel. This is useful in cases where two microphones are used in the system, but they may be located in different places of the final equipment and require different dynamic characteristics for optimal system operation.

Stereo Audio DAC

The AMT4432 includes a stereo audio DAC supporting sampling rates from 8 to 96KHz. Each channel of the stereo audio DAC consists of a digital audio processing block, a digital interpolation filter, a multi-bit digital delta-sigma modulator, and an analog reconstruction filter. The DAC is designed to provide improved performance at low sampling rates by increasing oversampling and matrix filtering, thereby keeping the quantization noise generated in the delta-sigma modulator and the signal matrix strongly suppressed in the audio range beyond 20KHz. This is achieved by maintaining a constant oversampling frequency of 128 × $f_{S(ref)}$ and changing the oversampling factor as the input sampling

frequency changes. With an $f_{S(ref)}$ of 48KHz, the digital delta-sigma modulator always operates at 6.144MHz. This ensures that the quantization noise generated by the delta-sigma modulator is low in the bandwidth below 20KHz at all sampling rates. Similarly, at $f_{S(ref)}$ = 44.1KHz, the digital delta-sigma modulator always operates at 5.6448MHz.

Digital Audio Processing for Playback

The DAC channel consists of optional filters for de-emphasis and bass, treble, midrange level adjustment,
speaker equalization, and 3-D effects processing. The de-emphasis function is implemented by a programmable
digital filter block with fully programmable coefficients. If de-emphasis is not required in a particular application, this programmable filter block can be
used for some other purpose. The de-emphasis filter transfer function is given by:

$$H(z) = \frac{N0 + N1 \times z^{-1}}{32768 - D1 \times z^{-1}}$$

In addition to the de-emphasis filter block, the DAC digital effects processing includes a fourth order digital IIR filter with programmable coefficients (one set per channel). This filter is implemented as cascade of two biquad sections with frequency response given by:

$$\left(\frac{N0 + 2 \times N1 \times z^{-1} + N2 \times z^{-2}}{32768 - 2 \times D1 \times z^{-1} - D2 \times z^{-2}}\right)\left(\frac{N3 + 2 \times N4 \times z^{-1} + N5 \times z^{-2}}{32768 - 2 \times D4 \times z^{-1} - D5 \times z^{-2}}\right)$$

Audio Analog Inputs

The AMT4432 includes ten analog audio inputs that can be configured as up to four fully differential pairs plus one single-ended pair of audio inputs, or as up to six single-ended audio inputs. These pins are connected via series resistors and switches to the virtual ground terminals of two fully differential op amps (one per ADC/PGA channel). By choosing to enable only one set of switches per op amp at a time, the inputs can be effectively multiplexed to each ADC/PGA channel. By choosing to enable multiple sets of switches per op amp at a time, mixing can also be achieved. Mixing multiple inputs can easily result in PGA output signals exceeding the range of the internal op amps, causing saturation and clipping of the mixed output signal. The user should take appropriate precautions when implementing mixing to avoid such saturation. In general, the mixed signal should not exceed $2V_{pp}$ (single-ended) or $4V_{pp}$ (differential).

Analog High Power Output Drivers

The AMT4432 includes four high-power output drivers with great flexibility. Each of these output drivers is capable of delivering 30mW into a 16ohm load in a single-ended configuration, and can be used in pairs connected in a bridged-load (BTL) configuration between the two driver outputs. The high-power output drivers can be configured in a variety of ways, including:

1. delivering up to two fully differential output signals;
2. delivering up to four single-ended output signals;
3. delivering two single-ended output signals, with one or two remaining drivers delivering a fixed VCM level for pseudo-differential stereo output.

Digital Microphone Connectivity

The AMT4432 supports connecting a digital microphone to the device by routing the digital signal directly to the ADC's digital decimation filter, where it is filtered, down-sampled, and transmitted to the host processor over the serial audio data bus. When digital microphone mode is enabled, the AMT4432 provides an oversampled clock output that the digital microphone uses to transmit data. The AMT4432 can latch data on the rising, falling, or both edges of this clock, providing support for stereo digital microphones.

Specifications

Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	AVDD_DAC to AVSS_DAC, DRVDD to DRVSS, AVSS_ADC	-0.3	3.9	V
	AVDD to DRVSS	-0.3	3.9	V
	IOVDD to DVSS	-0.3	3.9	V
	DVDD to DVSS	-0.3	3.9	V
	AVDD_DAC to DRVDD	-0.1	0.1	V
Digital input voltage	to DVSS	-0.3	IOVDD + 0.3	V
Analog input voltage	to AVSS_ADC	-0.3	AVDD + 0.3	V
Operation Temperature		-40	85	°C
Junction Temperature, T_J			105	°C
Storage Temperature, T_{STG}		-65	105	°C

ESD Ratings

		VALUE	UNIT
Electrostatic discharge $V_{(ESD)}$	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001	±1900	V
	Charged-device model (CDM), per JEDEC specification JESD22-VC101	±1500	V

Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Analog supply	2.7	3.3	3.6	V
Digital core supply voltage	1.65	1.8	1.95	V
Digital I/O supply voltage	1.1	1.8	3.6	V
Analog full-scale 0dB input voltage (DRVDD1 = 3.3V)		0.707		V_{RMS}
Stereo line output load resistance	10			Kohm
Stereo headphone output load resistance	16			ohm
Digital output load capacitance		10		pF

Electrical Characteristics

At 25°C, AVDD_DAC, DRVDD, IOVDD = 3.3V, DVDD = 1.8V, f_S = 48KHz, 16-bit audio data (unless otherwise noted)

	TEST CONDITIONS	MIN	NOM	MAX	UNIT
AUDIO ADC					
Input signal level (0-dB)	Single-ended input		0.707		V_{RMS}
Signal-to-noise ratio, A-weighted	f_s = 48ksps, 0-dB PGA gain, inputs ac-shorted to ground	80	92		dB
Dynamic range	f_s = 48ksps, 0-dB PGA gain, –60dB full-scale input signal		91		dB
Total harmonic distortion	f_s = 48ksps, 0-dB PGA gain, –2dB full-scale, 1-KHz input signal		-88	-70	dB
Power supply rejection ratio	217-Hz signal applied to DRVDD		49		dB
	1-KHz signal applied to DRVDD		46		dB
Gain error	f_s = 48ksps, 0-dB PGA gain, –2dB full-scale, 1-KHz input signal		0.84		dB
Input channel separation	1-KHz, –2-dB full-scale signal, MIC3L to MIC3R		-86		dB
	1-KHz, –2-dB full-scale signal, MIC2L to MIC2R		-98		dB
	1-KHz, –2-dB full-scale signal, MIC2L to MIC2R		-75		dB
ADC programmable gain amplifier maximum gain	1-kHz input tone		59.5		dB
ADC programmable gain amplifier step size			0.5		dB
Input resistance	MIC1L/MIC1R inputs routed to single ADC, input mix attenuation = 0dB		20		Kohm
	MIC1L/MIC1R inputs routed to single ADC, input mix attenuation = 12dB		80		Kohm
	MIC2L/MIC2R inputs routed to single ADC, input mix attenuation = 0dB		20		Kohm
	MIC2L/MIC2R inputs routed to single ADC, input mix attenuation = 12dB		80		Kohm
	MIC3L/MIC3R inputs routed to single ADC, input mix attenuation = 0dB		20		Kohm
	MIC3L/MIC3R inputs routed to single ADC, input mix attenuation = 12dB		80		Kohm
Input level control minimum attenuation setting			0		dB
Input level control maximum attenuation setting			12		dB
Input signal level	Differential Input		1.414		V_{RMS}
Signal-to-noise ratio, A-weighted	f_s = 48ksps, 0-dB PGA gain, inputs ac-shorted to ground, differential mode		92		dB
Total harmonic distortion	f_s = 48ksps, 0-dB PGA gain, –2-dB full-scale 1-kHz input signal, differential mode		-91		dB
ANALOG PASS THROUGH MODE					
Input to output switch resistance, (rds_{ON})	MIC1/LINE1 to LINE_OUT		330		ohm
	MIC2/LINE2 to LINE_OUT		330		ohm
ADC DIGITAL DECIMATION FILTER, f_s = 48KHz					
Filter gain from 0 to 0.39 f_S			±0.1		dB
Filter gain at 0.4125 f_S			-0.25		dB
Filter gain at 0.45 f_S			-3		dB
Filter gain at 0.5 f_S			-17.5		dB
Filter gain from 0.55 f_S to 64 f_S			-75		dB
Filter group delay			17/f_S		s
MICROPHONE BIAS					
Bias voltage	Programmable setting = 2.0		2.0		V
	Programmable setting = 2.5	2.3	2.5	2.7	V
	Programmable setting = DRVDD		DRVDD		V
Current sourcing	Programmable setting = 2.5V		4		mA
AUDIO DAC – DIFFERENTIAL LINE OUTPUT, LOAD = 10Kohm					
Full-scale output voltage	0-dB input full-scale signal, output volume control = 0dB, output common-mode setting = 1.35V		1.414		dB
Signal-to-noise ratio, A-weighted	No input signal, output volume control = 0dB, output common-mode setting = 1.35V, f_S = 48KHz	90	102		dB
Dynamic range, A-weighted	–60 dB 1-KHz input full-scale signal, output volume control = 0dB, output common-mode setting = 1.35V, f_S = 48KHz		99		dB
Total harmonic distortion	0-dB 1-KHz input full-scale signal, output volume control = 0dB, output common-mode setting = 1.35V, f_S = 48KHz		-94	-75	dB
Power-supply rejection ratio	217-Hz signal applied to DRVDD, AVDD_DAC		77		dB
DAC channel separation	0-dB full-scale input signal between left and right Lineout		123		dB

DAC gain error	0-dB 1-KHz input full-scale signal, output volume control = 0dB, output common-mode setting = 1.35V, f_S = 48KHz		-0.4		dB
AUDIO DAC – SINGLE ENDED LINE OUTPUT, LOAD = 10Kohm					
Full-scale output voltage	0-dB input full-scale signal, output volume control = 0dB, output common-mode setting = 1.35V		0.707		V_{RMS}
Signal-to-noise ratio, A-weighted	No input signal, output volume control = 0dB, output common-mode setting = 1.35V, f_S = 48KHz		97		dB
Total harmonic distortion	0-dB 1-KHz input full-scale signal, output volume control = 0dB, output common-mode setting = 1.35V, f_S = 48KHz		84		dB
DAC gain error	0-dB 1-KHz input full-scale signal, output volume control = 0 dB, output common-mode setting = 1.35V, f_S = 48KHz		0.55		dB
AUDIO DAC – SINGLE ENDED HEADPHONE OUTPUT, LOAD = 16ohm					
Full-scale output voltage	0-dB input full-scale signal, output volume control = 0dB, output common-mode setting = 1.35V		0.707		V_{RMS}
Signal-to-noise ratio, A-weighted	No input signal, output volume control = 0dB, output common-mode setting = 1.35V, f_S = 48KHz		95		dB
	No input signal, output volume control = 0dB, output common-mode setting = 1.35V, f_S = 48KHz, 50% DAC current boost mode		96		dB
Dynamic range, A-weighted	–60-dB 1-kHz input full-scale signal, output volume control = 0dB, output common-mode setting = 1.35V, f_S = 48KHz		92		dB
Total harmonic distortion	0-dB 1-KHz input full-scale signal, output volume control = 0dB, output common-mode setting = 1.35V, f_S = 48KHz		-80	-65	dB
Power-supply rejection ratio	217-Hz signal applied to DRVDD, AVDD_DAC		41		dB
	1-kHz signal applied to DRVDD, AVDD_DAC		44		dB
DAC channel separation	0-dB full-scale input signal between left and right Lineout		84		dB
DAC gain error	0-dB 1-KHz input full-scale signal, output volume control = 0dB, output common-mode setting = 1.35V, f_S = 48KHz		-0.5		dB
AUDIO DAC – LINEOUT AND HEADPHONE OUT DRIVERS					
Output common mode	First option		1.35		V
	Second option		1.5		V
	Third option		1.65		V
	Fourth option		1.8		V
Output volume control max setting			9		dB
Output volume control step size			1		dB
DAC DIGITAL INTERPOLATION – FILTER f_S = 48 ksps					
Pass band		0		0.45 f_S	Hz
Pass-band ripple			±0.06		dB
Transition band		0.45 f_S		0.55 f_S	Hz
Stop band		0.55 f_S		7.5 f_S	Hz
Stop-band attenuation			65		dB
Group delay			21/f_S		s
DIGITAL I/O					
Input low level		-0.3		0.3xIOVDD	V
Input high level	IOVDD > 1.6 V	0.7xIOVDD			V
	IOVDD < 1.6 V	1.1			V
Output low level				0.1xIOVDD	V
Output high level		0.8xIOVDD			V
POWER CONSUMPTION, DRVDD, AVDD_DAC = 3.3 V, DVDD = 1.8 V, IOVDD = 3.3 V					
Current consumption	IDRVDD+IAVDD_DAC	RESET held low		0.1		µA
	IDVDD			0.2		µA
	IDRVDD+IAVDD_DAC	Mono ADC record, f_S = 8kSPS, I2S slave, AGC off, no signal		2.1		mA
	IDVDD			0.5		mA
	IDRVDD+IAVDD_DAC			4.1		mA
	IDVDD			0.6		mA
	IDRVDD+IAVDD_DAC	Stereo ADC record, f_S = 48kSPS, I2S slave, AGC off, no signal		4.3		mA
	IDVDD			2.5		mA
	IDRVDD+IAVDD_DAC	Stereo DAC playback to line out, analog mixer bypassed, fS = 48kSPS, I2S slave		3.5		mA
	IDVDD			2.3		mA
	IDRVDD+IAVDD_DAC	Stereo DAC playback to line out, f_S = 48kSPS, I2S slave, no signal		4.9		mA
	IDVDD			2.3		mA

	IDRVDD+IAVDD_DAC	Stereo DAC playback to stereo single-ended headphone, f_S = 48kSPS, I2S slave, no signal		6.7		mA
	IDVDD			2.3		mA
	IDRVDD+IAVDD_DAC	Stereo line in to stereo line out, no signal		3.1		mA
	IDVDD			0		mA
	IDRVDD+IAVDD_DAC	Extra power when PLL enabled		1.4		mA
	IDVDD			0.9		mA
	IDRVDD+IAVDD_DAC	All blocks powered down, headset detection enabled		28		µA
	IDVDD			2		µA

Typical Characteristics

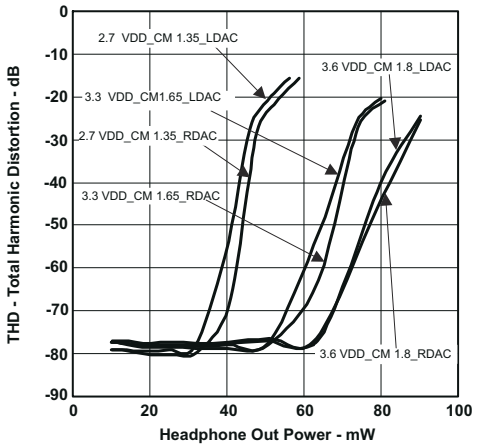


Figure 2-1. Total Harmonic Distortion vs Headphone Out Power

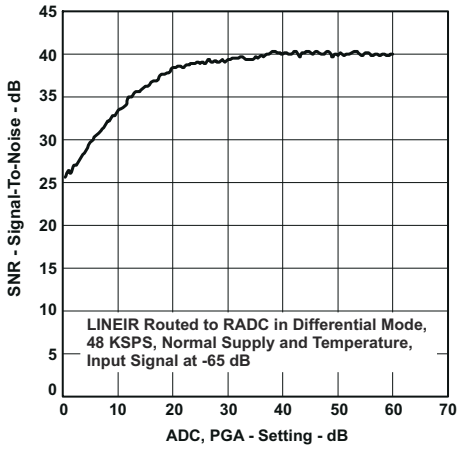


Figure 2-2. Signal-To-Noise Ratio vs ADC PGA Setting

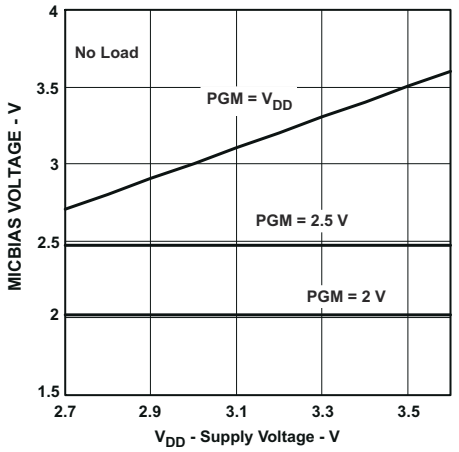


Figure 2-3. MICBIAS Voltage vs Supply Voltage

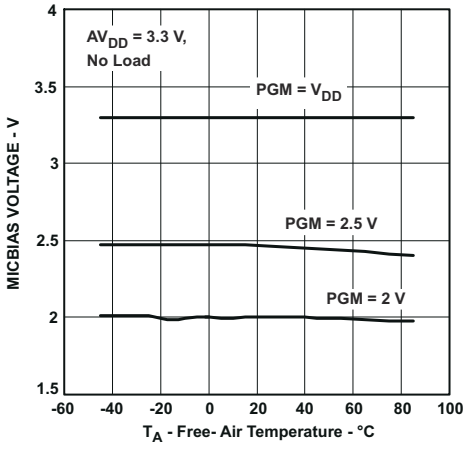


Figure 2-4. MICBIAS Voltage vs Free-Air Temperature

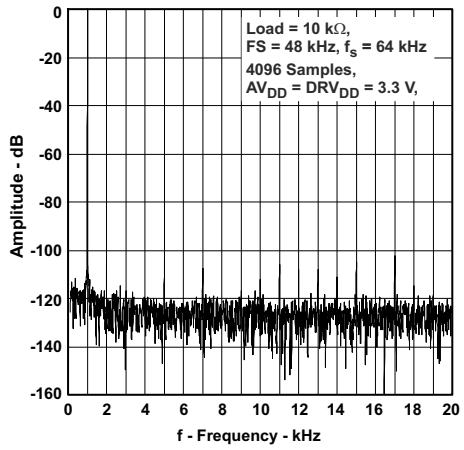


Figure 2-5. Left DAC FFT

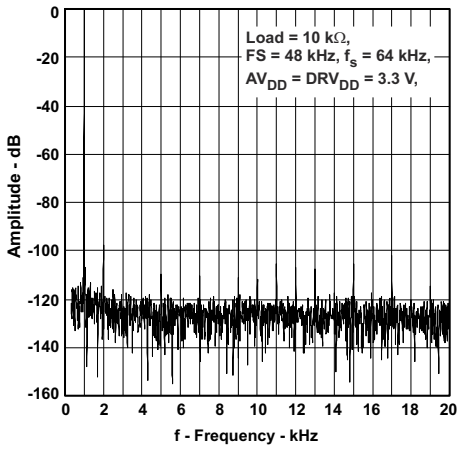


Figure 2-6. Right DAC FFT

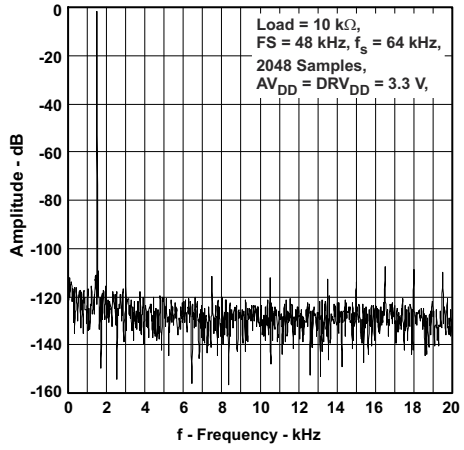


Figure 2-7. Left ADC FFT

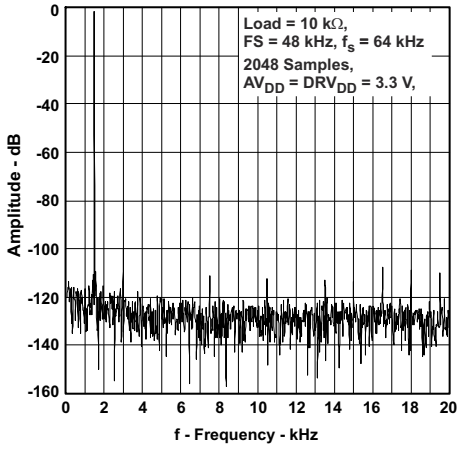


Figure 2-8. Right ADC FFT

Package information

UFQFPN48 package information

Figure 3. UFQFPN48 - 32-pin, 7x7 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline

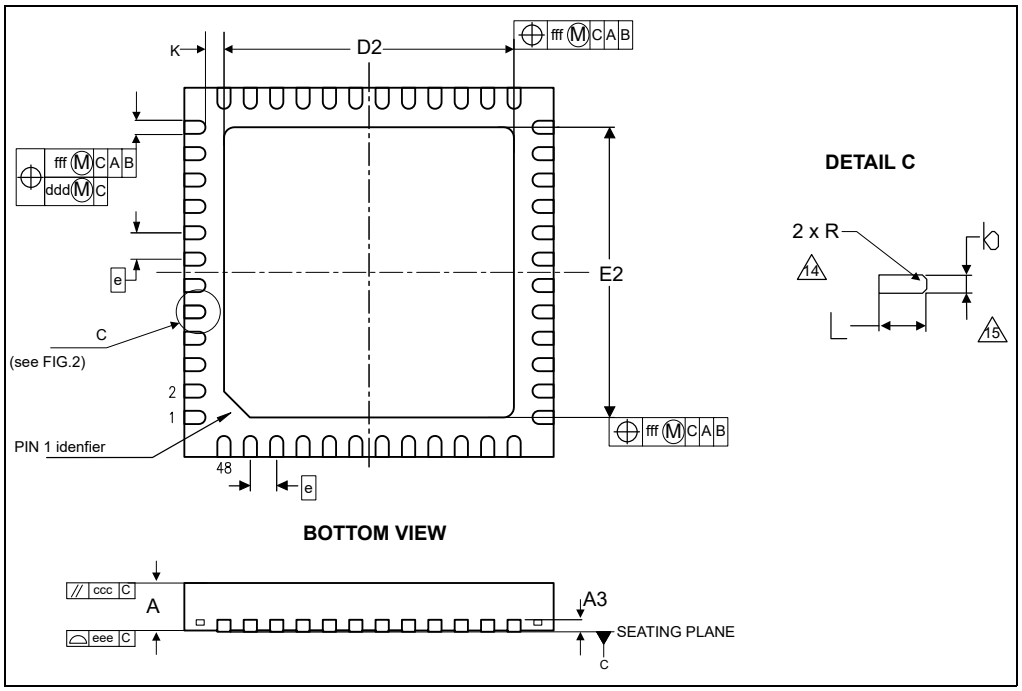
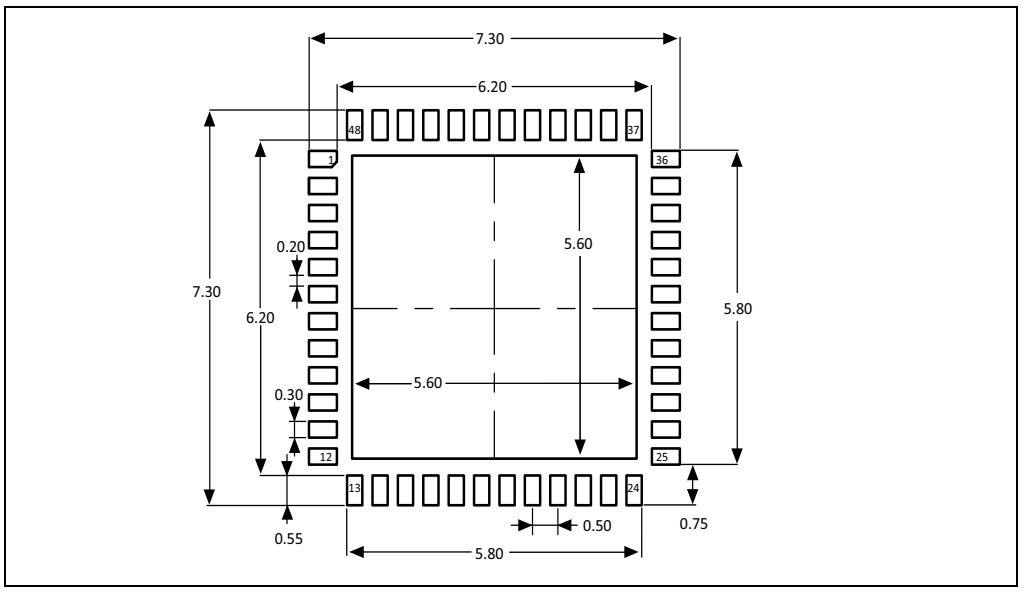


Table 1. UFQFPN48 - 48-pin, 7x7 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	-	-	0.050	-	-	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
D		7.000			0.2756	
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E		7.000			0.2756	
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
e	-	0.500	-	-	0.0197	-
L	0.300	-	0.500	0.0118	-	0.0197
ddd	-	0.050	-	-	0.0020	-

Figure 4. UFQFPN48 - 48-pin, 7x7 mm, 0.5 mm pitch ultra thin fine pitch quad flat package recommended footprint



Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location. Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 5. UFQFPN48 marking (package top view)