AMT Semiconductors Ltd.

AMT3447

Ultra-low-power Sound Processor with 16 APU (audio processing unit).

Features

- Ultra-low-power
  - 1.74V to 3.59V power supply
  - -40°C to 125°C temperature range
  - 30nA Standby mode
  - 84µA/MHz run mode
- Core: Arm® 32-bit Cortex®-M4 CPU with DSP
- Audio Processing Unit
  - 16x Independent APUs with DMA
- Clock Sources
  - 4 to 48 MHz crystal oscillator
  - 32 kHz crystal oscillator for RTC
- Memories
  - Up to 256KB single bank Flash, proprietary code readout protection
  - 64 KB of SRAM
  - AES Bootloader
- Communication interfaces
  - 1x I2S (audio interface)
  - 1x I2C
  - 2x UARTs
- DMA controller

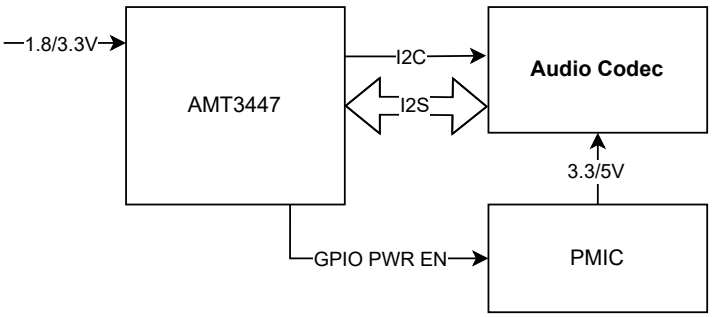
Description

The AMT3447 device are the ultra-low-power microcontroller with 16 independent APU. Each can be used as programmable filters for the audio record path.

Device Information

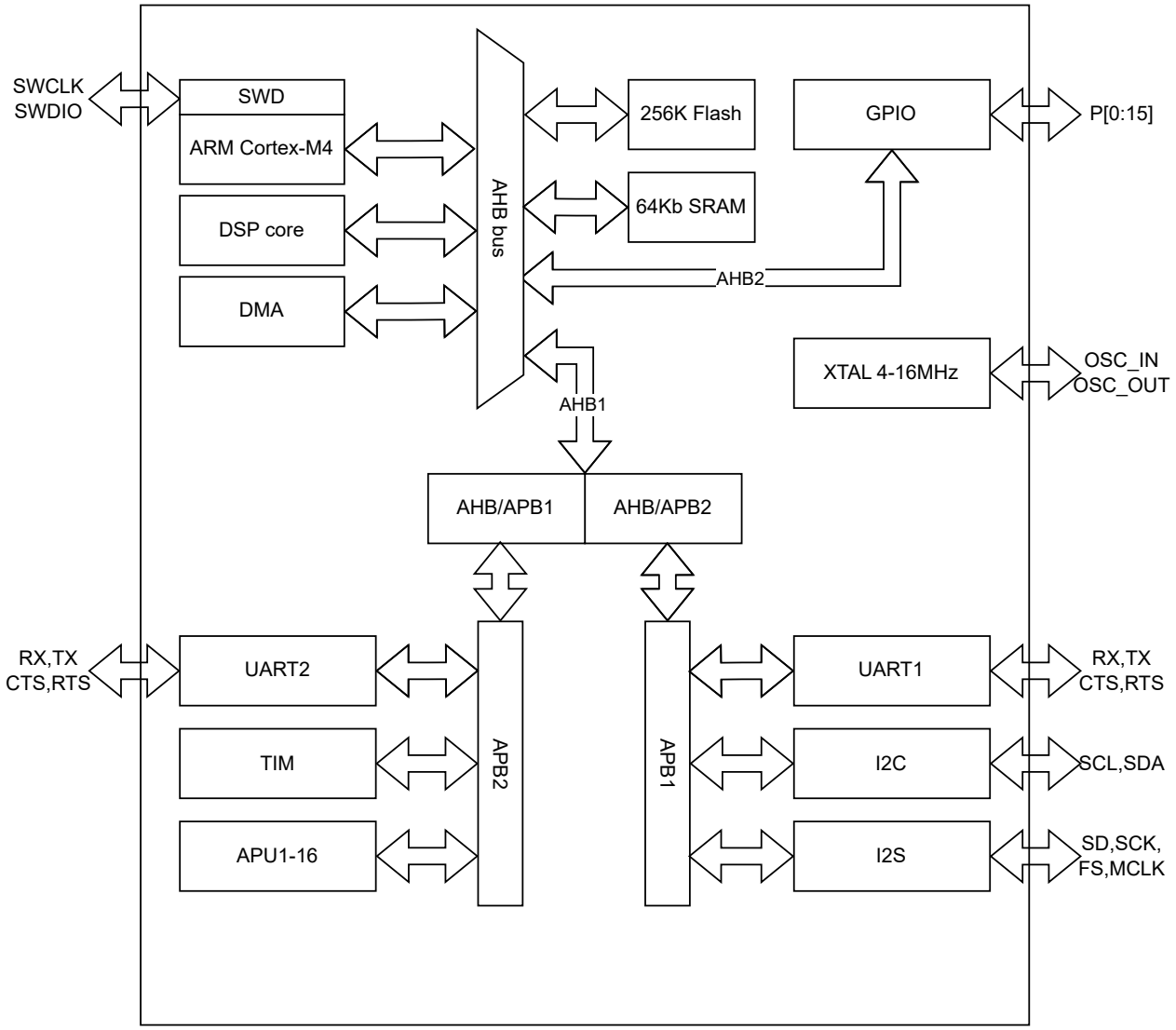
Part Number	Package	Size, mm
AMT3447	UFQFPN-32	5x5

Typical Application



AMT3447 Functional Diagram

Figure 1. AMT3447 block diagram



Functional Overview

Arm® Cortex®-M4 core with FPU

The Arm® Cortex®-M4 with FPU processor is the latest generation of Arm® processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Embedded Flash memory

AMT3447 devices feature 256 Kbyte of embedded Flash memory available for storing programs and data in single bank architecture. The Flash memory contains 128 pages of 2 Kbyte.

Embedded SRAM

AMT3447 devices feature 64 Kbyte of embedded SRAM.

Power supply management

VDD = 1.74 to 3.59 V: external power supply for I/Os (VDDIO1), the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through VDD pins.

Direct memory access controller (DMA)

The device embeds 1 DMA.

Direct memory access (DMA) is used in order to provide high-speed data transfer between peripherals and memory as well as memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps CPU resources free for other operations.
The DMA controller has 7 channels in total, each dedicated to managing memory access requests from one or more peripherals. Each has an arbiter for handling the priority between DMA requests.

General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. Fast I/O toggling can be achieved thanks to their mapping on the AHB2 bus.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

Timer

The AMT3447 includes one advanced control timer. Timer counter resolution is 16 bit.

Inter-integrated circuit interface (I2C)

The device embeds one I2C.

The I2C bus interface handles communications between the microcontroller and the serial I2C bus. It controls all I2C bus-specific sequencing, protocol, arbitration and timing.
The I2C peripheral supports:

- I2C-bus specification and user manual rev. 5 compatibility:
    - Slave and master modes, multimaster capability
    - Standard-mode (Sm), with a bitrate up to 100 kbit/s
    - Fast-mode (Fm), with a bitrate up to 400 kbit/s
    - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
    - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
    - Programmable setup and hold times
    - Optional clock stretching
- 1-byte buffer with DMA capability

Universal asynchronous receiver transmitter (UART)

The AMT3447 devices have one embedded universal asynchronous receiver transmitter (UART1).
This interface provides asynchronous communication, multiprocessor communication mode, single-wire half-duplex communication mode. They provide hardware management of the CTS and RTS signals, and RS485 Driver Enable. They are able to communicate at speeds of up to 10Mbit/s.
UART has a clock domain independent from the CPU clock, allowing to wake up the MCU from Stop mode using baud rates up to 204 Kbaud. The wake up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

The UART interface can be served by the DMA controller.

Inter-Integrated Circuit Sound (I2S)

The device embeds one I2S. The I2S bus interface handles communications between the microcontroller and the serial audio protocol.

The I2S peripheral supports:

- Two independent audio sub-blocks which can be transmitters or receivers with their respective FIFO.
- 8-word integrated FIFOs for each audio sub-block.
- Synchronous or asynchronous mode between the audio sub-blocks.
- Master or slave configuration independent for both audio sub-blocks.
- Clock generator for each audio block to target independent audio frequency sampling when both audio sub-blocks are configured in master mode.
- Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit.
- Peripheral with large configurability and flexibility allowing to target as example the following audio protocol: I2S, LSB or MSB-justified, PCM/DSP, TDM, AC’97 and SPDIF out.
- Up to 16 slots available with configurable size and with the possibility to select which ones are active in the audio frame.
- Number of bits by frame may be configurable.
- Frame synchronization active level configurable (offset, bit length, level).
- First active bit position in the slot is configurable.
- LSB first or MSB first for data transfer.
- Mute mode.
- Stereo/Mono audio frame capability.
- Communication clock strobing edge configurable (SCK).
- Error flags with associated interrupts if enabled respectively.
    - Overrun and underrun detection.
    - Anticipated frame synchronization signal detection in slave mode.
    - Late frame synchronization signal detection in slave mode.
    - Codec not ready for the AC’97 mode in reception.
- Interruption sources when enabled:
    - Errors.
    - FIFO requests.
- DMA interface with 2 dedicated channels to handle access to the dedicated integrated
- FIFO of each I2S audio sub-block.

Audio Processing Unit

The device embeds 16 independent APUs.

Each APUs can be used as a programmable audio filter. Processing includes a fourth order digital IIR filter with programmable coefficients (one set per channel). This filter is implemented as cascade of two biquad sections with frequency response given by:

$$\left(\frac{N0 + 2 \times N1 \times z^{-1} + N2 \times z^{-2}}{32768 - 2 \times D1 \times z^{-1} - D2 \times z^{-2}}\right)\left(\frac{N3 + 2 \times N4 \times z^{-1} + N5 \times z^{-2}}{32768 - 2 \times D4 \times z^{-1} - D5 \times z^{-2}}\right)$$

The N and D coefficients are fully programmable, and the entire filter can be enable.

The APU supports:

- Biquad Notch
- Biquad High Shelf
- Biquad Low Shelf
- Biquad HighPass
- Biquad LowPass
- Biquad AllPass
- Biquad BandPass Peak
- Biquad BandPass Skirt
- Biquad Peak

Specifications

Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input voltage VDD to VSS	-0.3	4	V
Operation Temperature	-40	125	°C
Junction Temperature, T_J	150	150	°C
Storage Temperature, T_{STG}	-65	150	°C

ESD Ratings

		VALUE	UNIT
Electrostatic discharge $V_{(ESD)}$	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001	±1900	V
	Charged-device model (CDM), per JEDEC specification JESD22-VC101	±1500	V

Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Voltage supply	1.74	3.3	3.59	V
Power dissipation at TA = 105 °C			523	mW
Total current into sum of all VDD power lines			140	mA
Total output current sunk by sum of all I/Os and control pins			100	mA

Package information

UFQFPN32 package information

Figure 2. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline

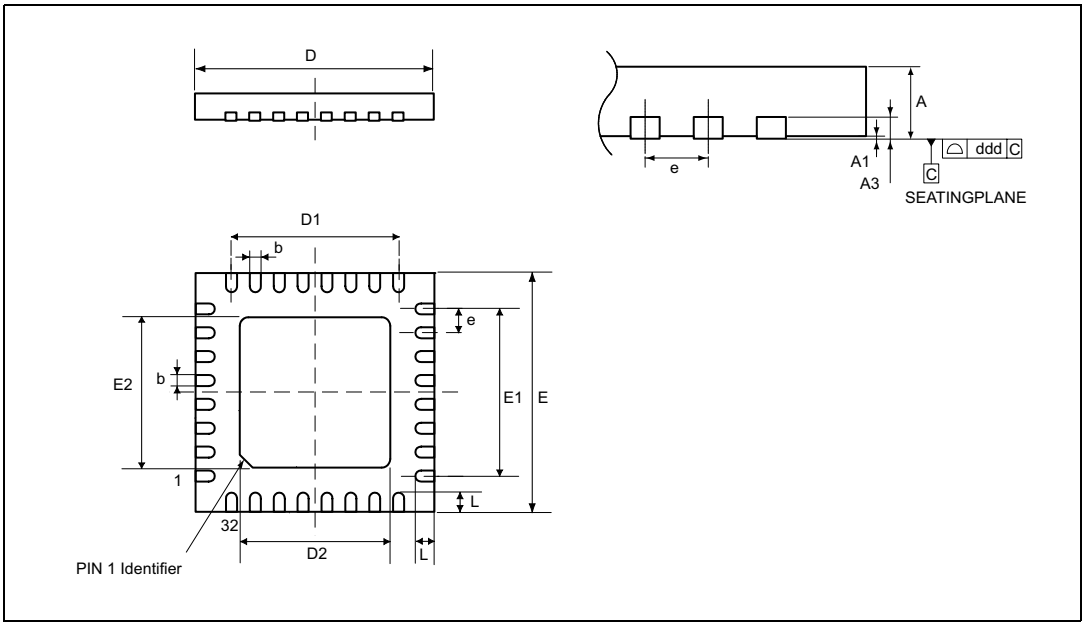
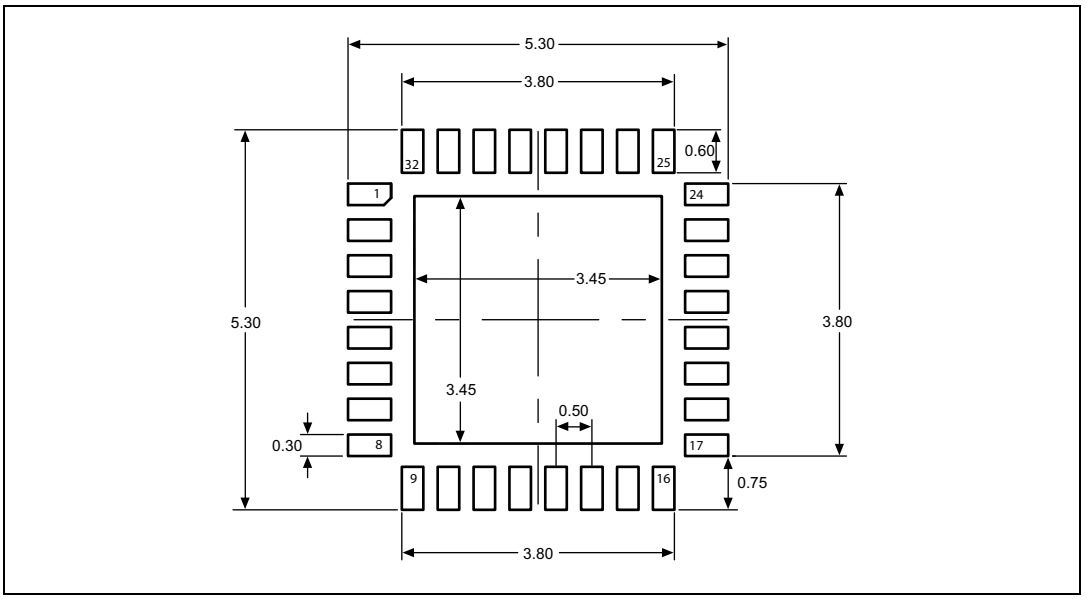


Table 1. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	-	-	0.050	-	-	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.180	0.230	0.280	0.0071	0.0091	0.0110
D	4.900	5.000	5.100	0.1929	0.1969	0.2008
D1	3.400	3.500	3.600	0.1339	0.1378	0.1417
D2	3.400	3.500	3.600	0.1339	0.1378	0.1417
E	4.900	5.000	5.100	0.1929	0.1969	0.2008
E1	3.400	3.500	3.600	0.1339	0.1378	0.1417
E2	3.400	3.500	3.600	0.1339	0.1378	0.1417
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

Figure 3. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package recommended footprint



Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location. Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 4. UFQFPN32 marking (package top view)